REMARKS

In response to the Office Action mailed January 16, 2003, the Applicant respectfully requests reconsideration.

IN THE WRITTEN DESCRIPTION

To further the prosecution of this application, amendments have been made to the written description of the specification as illustrated in the attachment hereto titled "Marked-Up Written Description". No new matter has been added by these amendments. The Examiner is respectfully requested to approve these amendments.

IN THE CLAIMS

To further the prosecution of this application, amendments have been made in the claims, as illustrated in the attachment hereto titled "Marked-up Claims."

Claims 13-20 were previously pending in this application. By this amendment, Applicants amend claims 13, 15, 16, 19, 20 and add claims 21-42. As a result, claims 13-42 are pending for examination, of which claims 13 and 25 are independent.

Added independent claim 25 is not a narrowing amendment to any of the originally filed independent claims, but claims a distinct aspect of the invention disclosed in the application.

1. Claims 13-24 Patentably Distinguish Over Zambrano

Claims 13-20 stand rejected under 35 U.S.C. §102(b) as purportedly being anticipated by U.S. Patent No. 5,489,799 (Zambrano). Applicants respectfully traverse this rejection.

1.1 Discussion of Zambrano

Zambrano is directed to an integrated edge structure for high voltage semiconductor devices and a related manufacturing process. (Col. 1, lines 9-11). Deep edge structures can be obtained that spread over regions sufficiently wide so as to decrease the electric field below a critical value. (Col. 2, lines 42-45).

Zambrano discloses that an edge structure includes two annular regions (4, 8) that are in contact with one another and that prevent a base-collector junction of a bipolar power transistor from experiencing early breakdowns induced by finite curvature radius under reverse bias. (Col.

3, lines 50-54; Col. 4, lines 8-12; Figs. 1 and 2). The edge structure (4,8) also may be used for a high voltage diode structure. (Col. 5, line 59 – col. 5, line 67; Figs. 6 and 7).

Contrary to the assertions of the Office Action, Zambrano fails to disclose that either of the annular rings (4 or 8) of the edge structure are closer to an integrated device (i.e., either the bipolar power transistor of Figs. 1 and 2 or the diode of Figs. 6 and 7) than the other. In fact, Figs. 1, 2, 6 and 7 illustrate that annular rings 4 and 8 both are in contact with the integrated device. Consequently, Zambrano does not disclose that an annular ring closer to the integrated device has a deeper depth than a farther away annular ring.

1.2. Claim 13 is Not Anticipated By Zambrano

Claim 13 has been amended merely for clarification, not in response to the §102(b) rejection or any art of record.

Claim 13 is not anticipated by Zambrano because Zambrano fails to disclose an integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns disposed in said number of superimposed semiconductor layers, wherein, **for each column of the at least two columns, the column is deeper than each column of the at least two columns that is farther from said high voltage semiconductor device than the column**, as recited in claim 13.

As discussed above, Zambrano fails to disclose that either of the annular rings of an edge structure are closer to an integrated device than the other, and, consequently, does not disclose that that an annular ring closer to the integrated device is deeper than a annular ring farther from the integrated circuit.

Therefore, for at least these reasons, claim 13 is not anticipated by Zambrano. Accordingly, Applicants respectfully request that the rejection of claim 1 under §102(b) as being anticipated by Zambrano be withdrawn.

Claims 14-24, which each depend directly or indirectly from claim 13, are patentable over the art of record for at least the same reasons as claim 13. Accordingly, Applicants respectfully request that the rejections of claims 14–20 under §102(b) as being anticipated by Zambrano be withdrawn.

2. Added Claims 25-42 Patentably Distinguish Over the Art of Record

Claim 25 patentably distinguishes over the art of record, including Zambrano, because the art of record does not disclose or suggest an edge structure integrated with a semiconductor device in an integrated circuit, the edge structure comprising: a plurality of regions of one or more vertically superimposed sub-regions of a first conductivity type, **each region laterally spaced from any other regions of the plurality of regions**, each region disposed a respective lateral distance from the semiconductor device, and each region having a depth relative to a surface of the integrated circuit, wherein, **for each region of the plurality of regions, a depth of a deepest sub-region of the region is deeper than a depth of a deepest sub-region of any other region of the plurality of regions that is disposed a farther lateral distance from the semiconductor device than the region is disposed**, as recited in claim 25.

As discussed above, Zambrano fails to disclose that either of the annular rings of an edge structure are closer to an integrated device than the other, and, consequently, does not disclose that that an annular ring closer to the integrated device is deeper than a annular ring farther from the integrated circuit.

Further, Zambrano discloses that the two annular regions are in contact with one another, as opposed to spaced apart.

Therefore, for at least these reasons, claim 25 is patentable over the art of record. Accordingly, Applicants respectfully submit that claim 25, and claims 26-42, which each depend directly or indirectly from claim 25, are in condition for allowance.

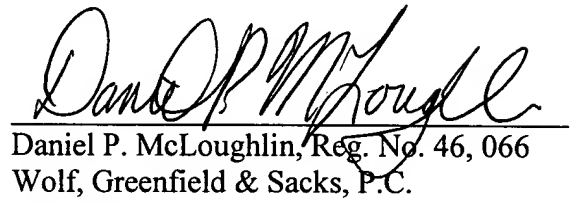
CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee

occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted
Frisina, et al., Applicant(s)

By: 

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MARKED-UP WRITTEN DESCRIPTION

Please rewrite the paragraph beginning on page 1, line 21 to read as follows:

A depletion region is associated with the PN junction, which can be considered as made up of two regions, a first one along the plane portion of the junction, a second one at the edges of said plane portion. The electric field has a different behavior in the two regions. In the plane portion the equipotential lines are parallel to the junction, the maximum electric field is located at the junction and the breakdown occurs when it reaches the critical value E_{CR}. At the junction edges, because of the finite junction depth, the equipotential lines are curved, and spaced closer together than in the plane portion. As a consequence, the electric field increases, and higher electric fields are associated with smaller curvature radii, i.e. a shallower junction. The breakdown voltage of [a] the edge portion of the PN diffused junction is usually lower than that of the corresponding plane portion of the junction, since the electric field in the edge region is much higher. The ratio between the breakdown voltage of the edge and the plane portion is thus below unity.

Please rewrite the paragraph beginning on page 5, line 13 to read as follows:

As an alternative, instead of performing, into each of the epitaxial layers 2 and 3 a single implant, several implants can be performed in succession into each of the epitaxial layers 2 and 3. Each implant of the succession is performed with a respective energy, so as to locate the peak dopant concentration at a respective depth. The dose of these implants ranges from [form] 5 x 10^{12} to 5 x 10^{13} atoms/cm^2, and the energies range from 100 keV to 900 keV or more. For example, where the implanted dopant is boron, three implants at 300 keV, 600 keV and 900 keV can be performed, so as to have peak dopant concentrations located at a depth of 0.7 μm, 1.2 μm and 1.7 μm, respectively.

Please rewrite the paragraph beginning on page 7, line 14 to read as follows:

It is evident that the number of N type semiconductor layers can be different from six and so can that of the P doped regions inside them, depending on the overall thickness of the drain layer of the final device, i.e., on the voltage to be sustained by the power device.

MARKED-UP CLAIMS

13. (Amended) An integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns [being inserted] disposed in said number of superimposed semiconductor layers, wherein, for each column of the at least two columns, the column is [the column near said high voltage semiconductor device being] deeper than each column of the at least two columns that is [the column] farther from said high voltage semiconductor device than the column.

15. (Amended) The integrated edge structure according to claim 13, wherein said number of superimposed semiconductor layers is superimposed [to] on a semiconductor substrate.

16. (Amended) The integrated edge structure according to claim 13, wherein each one of said at least two columns has a depth decreasing by shifting from said high voltage semiconductor device towards [the] an outside of the integrated edge structure.

19. (Amended) The integrated edge structure according to claim 13, wherein said first conductivity type [of conductivity] is [the] N type and said second conductivity type [of conductivity] is [the] P type.

20. (Amended) The integrated edge structure according to claim 13, wherein said first conductivity type [of conductivity] is [the] P type and said second conductivity type of conductivity is [the] N type.